IN THE SPECIFICATION:

Please insert the following title at the beginning of the specification:

-- METHOD AND APPARATUS FOR TRANSFERRING DATA BETWEEN A SLOWER CLOCK DOMAIN AND A FASTER CLOCK DOMAIN IN WHICH ONE OF THE CLOCK DOMAINS IS BANDWIDTH LIMITED --

Please replace the paragraph appearing on page 18, lines 7-18 of the specification, with the following amended paragraph:

-- A method and apparatus is provided for ensuring the integrity of data being transferred between two clock domains. Data is transferred on every clock signal from a faster clock domain to a slower clock domain. ~~in which one clock domain is a faster clock domain than the other clock domain in which data is transferred on every clock signal from the slower clock domain. Data is received at a data collection or data capture unit for transfer to the second clock domain. The data received has a first data size and is stacked with additional data of the first data size to generate data having a second data size. For example, the first data size may be 16 bits while the second data size is 32 bits.~~ Data is collected by the data capture unit in two or more banks of registers for transfer to the second clock domain. The data collected has a first data size and is stacked with additional data of the first data size to generate data having a second data size. When two banks of registers are used, one bank of registers is being filled while the other bank of registers is passing data to the second clock domain. These two banks of registers provide two data paths to the synchronization logic for the second clock domain. This is especially advantageous when the limit of available bandwidth has been reached by one of the clock domains. --